CLAIMS:

We claim:

1. An apparatus comprising:

an amplifier to generate an output to a load; and

a digital-to-analog converter to drive the amplifier during at least one of powering up and powering down the amplifier, the digital-to-analog converter to control the amplifier to ramp the voltage at the output at a predetermined rate to reduce rapid voltage changes from being sent to the load during the at least one of powering up or powering down of the amplifier.

2. The apparatus of claim 1 wherein the output of the amplifier to the load is through a blocking capacitor, the digital-to-analog converter to control the ramp of the voltage at the output to at least one of charging the blocking capacitor to a steady-state reference value at the predetermined rate and of discharging the blocking capacitor from the steady-state reference value at the predetermined rate.

3. The apparatus of claim 2 wherein the amplifier to generate an audio output to the load in which the at least one of powering up and powering down at the predetermined rate reduces audio pop and click at the load.

4. The apparatus of claim 1 further comprises a control circuit to generate data sent to the digital-to-analog converter during at least one of powering up and powering down the amplifier.

5. The apparatus of claim 4 wherein the data from the control circuit ramps the voltage at a substantially linear ramp rate.

6. An apparatus comprising:

an audio amplifier to generate an output to an audio load;

a digital-to-analog converter to drive the audio amplifier during at least one of powering up and powering down the audio amplifier, the digital-to-analog converter to control the audio amplifier to ramp the voltage at the output at a predetermined rate to reduce audio pop and click from being heard at the load during the at least one of powering up or powering down of the audio amplifier; and

a control circuit to generate data sent to the digital-to-analog converter during at least one of powering up and powering down the audio amplifier.

7. The apparatus of claim 6 further comprises a clamping switch at an output node of the audio amplifier to clamp the node to a power return potential, wherein the clamping switch clamps the output node to the return potential at initiation of a powering up sequence and releases the clamp when the audio amplifier and the digital-to-analog converter are substantially fully powered.

8. The apparatus of claim 7 wherein the data from the control circuit ramps the voltage at a ramp rate below frequency heard at the load.

9. The apparatus of claim 6 further comprises a clamping switch at an output node of the audio amplifier to clamp the node to a power return potential, wherein the clamping switch clamps the output node to the return potential at initiation of a powering down sequence and releases the clamp when the audio amplifier and the digital-to-analog converter are substantially turned off.

10. The apparatus of claim 9 wherein the data from the control circuit ramps the voltage at a ramp rate below frequency heard at the load.

11. A method to power up or power down an audio amplifier comprising:

sending digital data for digital-to-analog conversion during a powering up or powering down of an audio amplifier, which generates an output to an audio load;

converting the digital data to drive the audio amplifier; and

using the converted digital data to control the ramping of the voltage at the output to not exceed a predetermined rate to reduce audio pop and click from being heard at the load during the powering up or powering down of the audio amplifier.

12. The method of claim 11 further comprises ramping the voltage at the output to a steady-state reference value at the predetermined rate during the powering up of the audio amplifier.

13. The method of claim 12 further comprises the clamping of an output node of the audio amplifier to a power return potential during powering up and releasing the clamp when the amplifier is substantially fully powered.

14. The method of claim 12 wherein using the converted digital data controls the ramping of the voltage to a ramp rate below frequency heard at the load.

15. The method of claim 11 further comprises ramping the voltage at the output from a steady-state reference value at the predetermined rate during the powering down of the audio amplifier.

16. The method of claim 15 further comprises the clamping of an output node of the audio amplifier to a power return potential during powering down and releasing the clamp when the amplifier is substantially turned off.

17. The method of claim 15 wherein using the converted digital data controls the ramping of the voltage to a ramp rate below frequency heard at the load.

18. An integrated circuit comprising:

an audio amplifier to generate an analog output to an audio load, when the audio load is operably coupled to the integrated circuit;

a digital-to-analog converter to drive the audio amplifier during at least one of powering up and powering down the audio amplifier, the digital-to-analog converter to control the audio amplifier to ramp the voltage at the output at a predetermined rate to reduce audio pop and click from being heard at the load during the at least one of powering up or powering down of the audio amplifier; and

a control circuit to generate data sent to the digital-to-analog converter during at least one of powering up and powering down the audio amplifier.

19. The integrated circuit of claim 18 wherein the control circuit is a digital signal processor.

20. The integrated circuit of claim 18 further comprises a clamping switch at an output node of the audio amplifier to clamp the node to a power return potential, wherein the clamping switch clamps the output node to the return potential at initiation of a powering up sequence and releases the clamp when the audio amplifier and the digital-to-analog converter are substantially fully powered.

21. The integrated circuit of claim 18 further comprises a clamping switch at an output node of the audio amplifier to clamp the node to a power return potential, wherein the clamping switch clamps the output node to the return potential at initiation of a powering down sequence and releases the clamp when the audio amplifier and the digital-to-analog converter are substantially turned off.